Amendments to the Specification:

Please replace the title with the following amended title:

ENERGY SAVING PASSIVE MATRIX DISPLAY DEVICE AND METHOD FOR DRIVING THE COLUMN VOLTAGE HAVING REDUCED TRANSITIONS

Please replace the paragraph beginning on page 1, line 15 with the following amended paragraph:

The display technique will play an increasingly important role in the information and communication technique in the years to come. Being an interface between humans and the digital world, the display device is of crucial importance for the acceptance of contemporary information systems. Notably portable apparatus such as, for example, notebooks, telephones, digital cameras and personal digital assistants cannot be realized without utilizing displays. The passive matrix LCD technology is a very commonly used display technology; it is used, for example in PDA's and in mobile telephones. Passive matrix displays are usually based on the (S)TN (Super Twisted Nematic) effect. A passive matrix LCD consists of a number of substrates. The display is subdivided in the form of a matrix of rows and columns. The row electrodes and column electrodes are arranged on respective substrates ~~und~~ and form a grid. A layer with liquid crystals is provided between said substrates. The intersections of these electrodes form pixels. These electrodes are supplied with voltages that orient the liquid crystal molecules of the driven pixels in an appropriate direction so that the driven pixel appears in a different brightness.

Please replace the paragraph beginning on page 2, line 17 with the following amended paragraph:

In order to drive the whole display, said calculation rule has to be calculated multiple times. This ~~requires an~~ requires intensive data processing and may--dependent

on the picture to be displayed--cause the column voltage signal to change very often. This in consequence means that the column driving signal will also have many transitions. The possibly high number of transitions of the column driving signal and the intensive data processing required has a negative impact on the overall power consumption of the driver.

Please replace the paragraph beginning on page 4, line 13 with the following amended paragraph:

In the following the structure of a grey scale table will be described. A grey scale table defines the pixel state ~~a_{ij}~~ $a_{i,j}$ for a certain sub selection time slot for all the combinations of sub selection time slots, frame/phases, and grey scales. I.e. in Table 1 the pixel state ~~a_{ij}~~ $a_{i,j}$ for grey scale GS 5 is defined as follows: in the first frame/phase the pixel state is always 1, in the second frame/phase the pixel state is only in the first sub selection time slot 1, for the three subsequent sub selection time slots of that frame/phase and the following frames/phases the pixel state is always 0. This means that a grey scale on a certain pixel is achieved by providing different pixel states over the number of frames/phases and sub selection time slots, whereby the change of the order of pixel states over the frames belonging to one and the same superframe does not influence the resulting and displayed grey scale on that certain pixel.

Please replace the paragraph beginning on page 5, line 3 with the following amended paragraph:

To solve the problem of flickering and high frame frequency a technique is used called phase mixing. In order to prevent visible artifacts like flickering especially at low frame frequencies it is necessary that grey scales in adjacent pixels are generated ~~with~~ with a different pattern or sequence of pixels states. For ~~generating~~ generating a different pattern for adjacent pixels this phase mixing method is applied. Phase mixing uses a set of tables, which are denoted as phase mixing tables that assign each pixel and frame a certain phase such that the phase of a particular pixel changes from frame to frame

without having twice the same value. For each phase and grey scale the grey scale table then defines the pixel state to sub selection time slot assignment to be used. By assigning adjacent pixels in the same frame to different phases, the pattern for generating grey scales can be altered. So by using phase mixing it is achieved that grey scales in adjacent pixels over a sequence of frames are generated with a different pattern. The phase which is used for a certain pixel increases by one for the following frame. Also other rules for changing the phase between frames may be used provided that for any pixel each phase is only used once within a superframe. Phase mixing can also be used for FRC only, hence without the combination with PWM.

Please replace the paragraph beginning on page 6, line 15 with the following amended paragraph:

The phase mixing tables in Table 2 define that e.g. during frame 0 the pixel $p_{0,1}$ (row index 0, column index 1) will be generated according to phase 2. Referring back to Table 1, this means that pixel $p_{0,1}$ will be driven based on the pixel states as specified in Table 1 for frame/phase 2. What this exactly means, will be explained now in more detail with an example: Given that pixel $p_{0,1}$ should be displayed with grey scale 5, and provided that the grey scale Table 1 and the phase mixing Table 2 are used, pixel $p_{0,1}$ will be driven in frame 0 according to phase 2. This means that pixel $p_{0,1}$ is driven in frame 0 four times with a pixel state of 0. In the next frame that is frame 1, pixel $p_{0,1}$ will be driven according to phase 3 and therefore with four times a pixel state of 0. In frame 2 pixel $p_{0,1}$ will be driven according to phase 0 and therefore with four times a pixel state of 1. Finally, in the last frame that is frame 3, pixel $p_{0,1}$ will be driven according to phase 1 and therefore with a pixel state of ~~once 0~~ once 1 and then three ~~times 1~~ times 0. Comparing this to pixel $p_{0,2}$ which is the next column neighbor to pixel $p_{0,1}$, it can be seen from Table 2 that this pixel is driven in all frames with phases differing from the ones of pixel $p_{0,1}$. Therewith and provided that pixel $p_{0,2}$ is also meant to be driven to grey scale 5, the pattern how the grey scales are generated will differ. As a consequence, flickering foremost at low frame frequencies can be reduced considerably.

Please replace the paragraph beginning on page 7, line 13 with the following amended paragraph:

The column voltage $G_j(t)$ for the duration a certain group of p ~~rows is~~ rows selected (row selection time) is calculated by using the equation or calculation rule below, wherein the column voltage $G_j(t)$ depends on the pixel states ~~a_{ij}~~ $a_{i,j}$ to be displayed in the respective column for the group of rows selected and on the set of orthogonal selection signals which are supplied to the p rows of the group,

$$G_j(t) = \frac{1}{\sqrt{N}}\{a_{0,j} * F_0(t) + a_{1,j} * F_1(t) + a_{2,j} * F_2(t) + a_{3,j} * F_3(t)\} \quad (1)$$

Please replace the paragraph beginning on page 7, line 20 with the following amended paragraph:

whereas Eq. (1) represents the column driving voltage ($G_j(t)$-function) for MRA with p=4 for the column with index j for the duration a certain group of p rows is selected and under the assumption that the row index i is given as the row number modulo 4. Note: ~~a_{ij}~~ $a_{i,j}$: pixel state of the pixel given by row_i and $column_j$ (pixel in its ON state: a_{ij}=-1 dec (chosen to be represented by 0 digital), pixel in its OFF state: a_{ij}=+1 dec (chosen to be represented by 1 digital)).

Please replace the paragraph beginning on page 18, line 21 with the following amended paragraph:

FIG. 7 shows a block diagram for generating the column voltages, which are provided to the column electrodes. The Block 71 shows a part of memory RAM. This RAM Slice 71 stores the pixel data for one column of the display. The pixel data for that column is supplied to the grey scale control block 72. The grey scale control block 72 stores the grey scale table and the phase mixing tables as for example depicted in Table 3 and FIG. 5. Based on these tables and the pixel data from the RAM Slice 71, the pixel

state ~~a_{ij}~~ $a_{i,j}$ (ON or OFF) of a certain pixel during a certain row sub selection time slot is derived. Additionally, this block 72 generates the necessary control signals for the Up/Mirror Control block 77, which is described below. The next block 73 is the $G_j(t)$-Function calculator, which is responsible for calculating the $G_j(t)$-function of the column voltage as given in Eq. (1). Its inputs are the pixel state ~~a_{ij}~~ $a_{i,j}$ from the GS-Control block 72 and the orthogonal function F_i which are provided from an external source that is not shown. This $G_j(t)$-function is provided to the Up/Mirror control 77 and the next block 74 that registers the $G_j(t)$-function with the beginning of the next row selection time. In the block 75 the $G_j(t)$-function which is represented by three signals, is incremented or decremented by one. The output of the incrementing/decrementing block 75 is supplied to the decoder 76. The decoder 76 decodes the coded column voltage level and activates the enable signal that corresponds to the column voltage level for driving the respective column. The Up/Mirror Control block 77 derives based on the output of the $G_j(t)$-Function calculator 73 and the control signals from the GS-Control block 72 as well as the current column level whether or not the waveform in the following row selection time needs to be mirrored or not. Based on this information and additional information obtained from the GS-Control block 72, the Up/Mirror Control block 77 controls the +1/-1 block 75 that increases or decreases whenever and as long as needed the column voltage by one level.